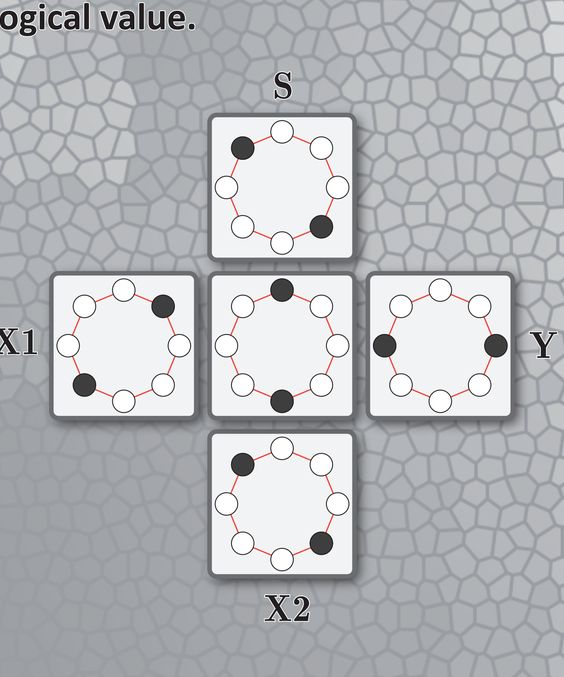
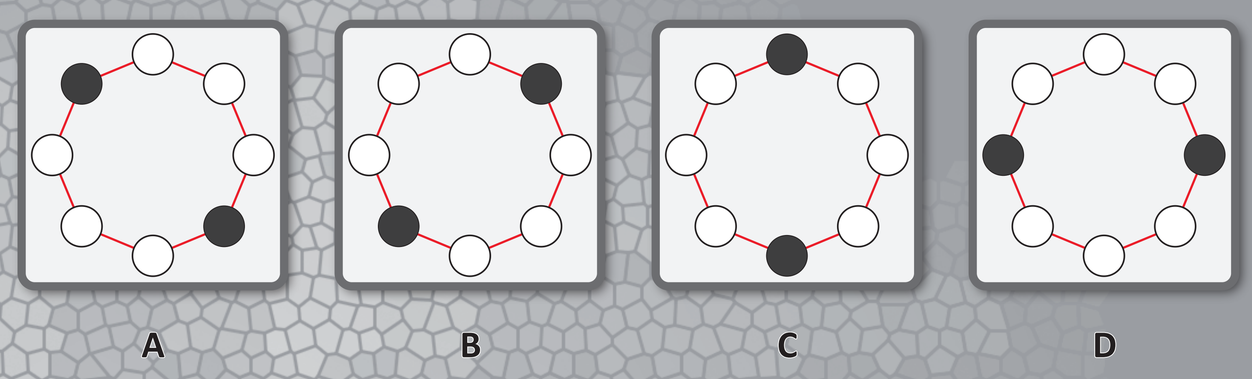
University of Ljubljana
Faculty of Computer and Information Science

Solving the ternary QCA logic gate problem by means of adiabatic switching

Primož **Pečar**
Miha **Mraz**
Nikolaj **Zimic**
Miha **Janež**
and Iztok **Lebar Bajec**

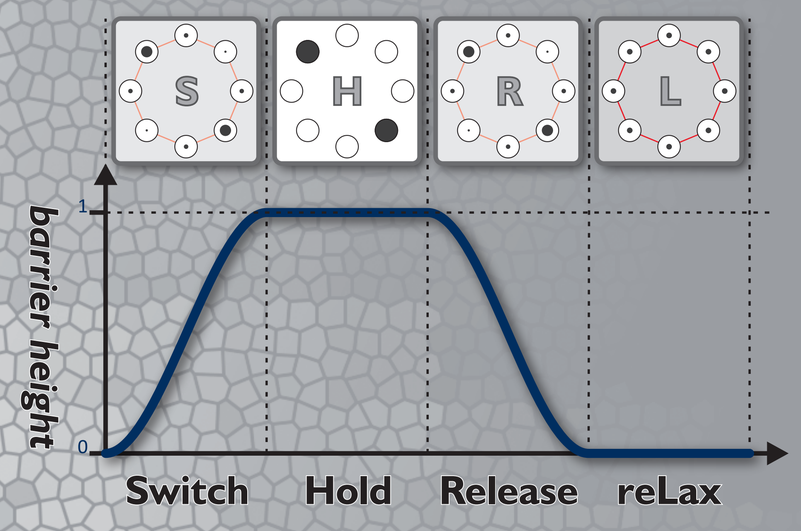




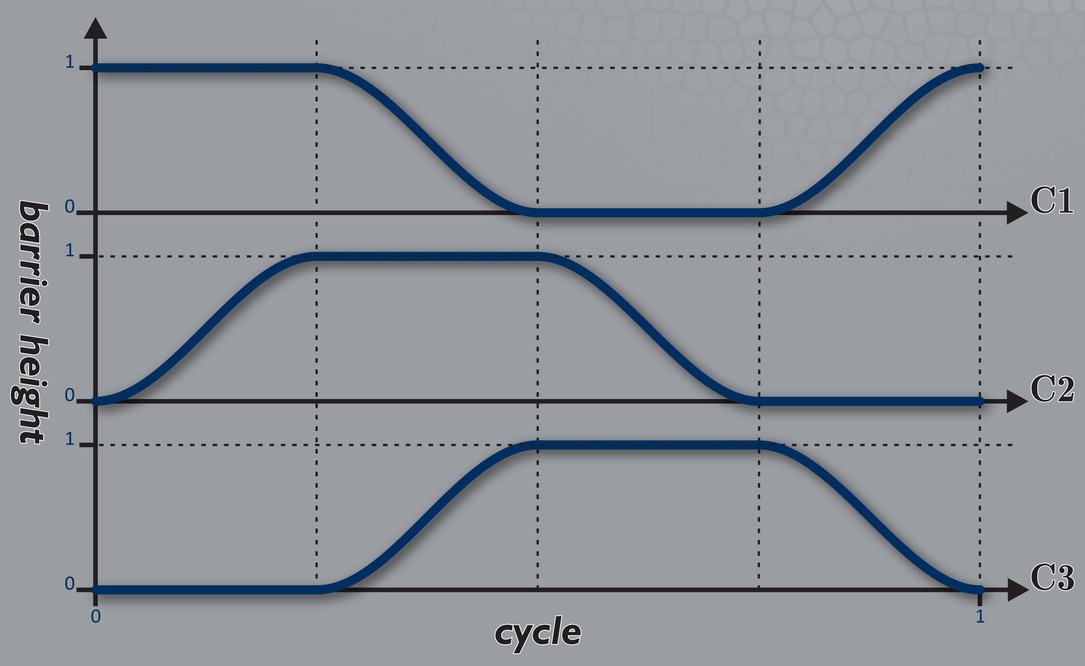
The geometry of the ternary quantum-dot cell. It is comprised of eight quantum dots with diameter D and occupied by two electrons. The near-neighbour distance between dot centers is 2D. Red lines denote tunneling paths, where *t* is the tunneling energy. The four distinctive but equivalent ground states of the ternary QCA cell. State A is interpreted as logic value 0, state B as logic value 1, state C as logic value 1/2, whereas state D is allowed only as an internal processing state and it can not be interpreted as a logical value.

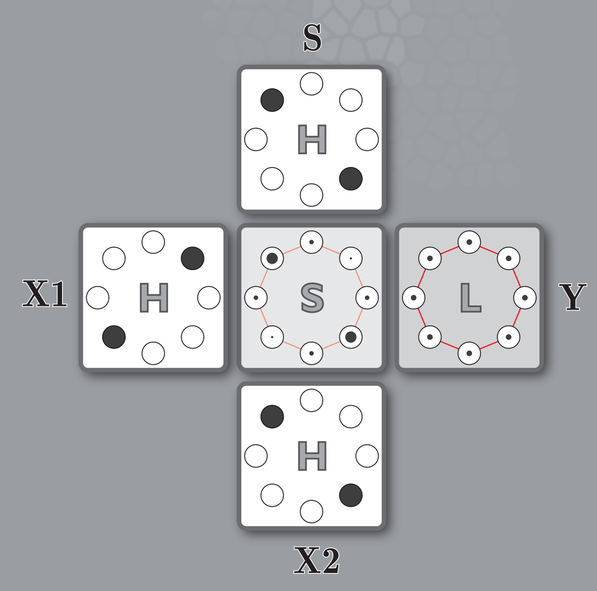
	S	X1	X2	S	X1	X2	Y	Y
AND(X1,X2)	0	0	0	A	A	A	A	0
	0	0	½	A	A	C	A	0
	0	0	1	A	A	B	A	0
	0	½	0	A	C	A	A	0
	0	½	½	A	C	C	C	½
	0	½	1	A	C	B	C	½
	0	1	0	A	B	A	D	0
	0	1	½	A	B	C	C	½
	0	1	1	A	B	B	B	1
OR(X1,X2)	1	0	0	B	A	A	A	0
	1	0	½	B	A	C	C	½
	1	0	1	B	A	B	D	1
	1	½	0	B	C	A	C	½
	1	½	½	B	C	C	C	½
	1	½	1	B	C	B	B	1
	1	1	0	B	B	A	B	1
	1	1	½	B	B	C	B	1
	1	1	1	B	B	B	B	1

The problematic structure comprised of three input cells S, X1 and X2, one internal cell and one output cell Y. As we can see in the table the structure behaves almost as the ternary AND or OR logic gates. There are only two erroneous outputs (ie. AND(1,0) and OR(0,1)).



The cyclic signal that controls interdot barriers has four phases. In the graph the barrier heights are normalized. The value 0 corresponds to low barriers; the confinemet of the electrons on the individual quantum dots is reduced. The value 1 corresponds to high barriers, which localizes the electrons on the individual quantum dots.





The basic geometry of the problematic structure is decomposed into three subsections, controlled by three phase shifted cyclic signals, denoted C1, C2 and C3. Signal C1 controls the input cells S, X1 and X2, signal C2 controls the internal cell and signal C3 controls the output cell. In this case the geometry works as intended, i.e. as ternary logic AND if either S, X1 or X2 is in state A and as ternary logic OR if either S, X1 or X2 is in state B.