Ternary Computing with Quantum Dots

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The recent years have witnessed a dramatic reduction in size coupled with the increase of speed in computing devices. Following this trend the current approaches will inevitably reach their limits, what calls for studies of alternative processing platforms. Presently the most promising one is the Quantum-dot Cellular Automaton (QCA), a processing platform based on interacting quantum dots. It was introduced by C. S. Lent in the mid 1990s. What followed was an exhilarating period with the development of a line and functionally complete set of logic structures, as well as more complex processing structures, however all in the realm of binary logic. Regardless of these achievements, it has to be acknowledged that the use of binary logic is in computing systems mainly the end result of the technological limitations, which the designers had to cope with in the early days of their design. Lebar Bajec et al., based on the argument that processing platforms of the future should not disregard the clear advantages of multi valued logic, first showed that the QCA can be used for ternary processing as well. The basic building block, a ternary QCA cell, is a planar structure comprising eight quantum dots and two electrons that can tunnel between neighboring dots. With this cell, which has four distinctive but equivalent ground states, three logic values can be represented. Based on the semi-classical modeling approach Lebar Bajec et al. showed that the line and the core of the inverter can be promoted to the ternary realm with a simple switch of the basic building block (i.e. binary QCA cell for its ternary counterpart). This, however, was not true for the geometry of the structure that implements the AND/OR logic gates.

The problem led us to the development of a more precise quantum-mechanical model based on the extended-Hubbard type Hamiltonian. Our simulations using parameter values as if the material in use was GaAs confirmed the known logic gate problem, as well as shown a few additional ones. The most obvious were erroneous behavior of the corner line, fan-out and inverter core with an extended output. Here we present a solution that is based on adiabatic switching, which ensures the modeled structure is in its ground state throughout the whole time of the switch. This is achieved by controlling the inter dot barriers with a cyclic signal consisting of four phases. This allows any arbitrary QCA structure to be decomposed into multiple subsections controlled by four distinct phase shifted signals, achieves the introduction of the synchronization of data transfer between subsections and allows bypassing the problems of the corner line and fan-out, as well as those of the inverter core and AND/OR logic gates. What is more, the architecture of the structures that implement the described ternary logic functions equals the one employed for the implementation of the binary counterpart. That opens up the possibility to design advanced ternary arithmetic-logic and memorizing units, the principal components of ternary processors. It has to be noted that in this work we assume that there are no technological limitations and neglect practical time scales of adiabatic switching principally in favor of focusing attention on processing architectures. Nevertheless, we are well aware of the implementation problems and for this reason the switching dynamics and material suitability are part of our current research directive.