Contribution (Oral/Poster/Keynote)

Two-layer synchronized ternary quantum-dot cellular automata wire crossings

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Since the first introduction of Quantum-dot Cellular Automata (QCA), an interesting nano-scale computing paradigm, by C. Lent et al. in 1993 [1], many researchers have embraced its simple concept and potential as a future processing platform. Soon QCAs that implement the functionally complete set of binary logic functions and from there on more and more complex designs were introduced.

In recent years a group of researchers have presented a generalization of the basic QCA cell (fig 1), namely the ternary QCA (tQCA) cell (fig 2) [2], which enables ternary computation. Their principal motivator was the premise that future processing platforms should not disregard the advantages of multi-valued processing. These have been extensively researched over the past five decades [3]. The group presented the basic ternary building blocks, the inverter, majority gate, wire, corner-wire and fan-out, and more recently also a functionally complete set of ternary logic functions, based on Post Logic, and a memorizing tQCA circuit [4,5].

Due to the specifics of the tQCA cell wire crossings seem to be the principal drawback before a more widespread acceptance of tQCA circuitry. Wire crossings are one of the most used steps in systematic logic design. In the classic, binary QCAs, wires can be crossed either in a coplanar fashion, by using rotated QCA cells for one of the wires, or in a multilayer fashion, where two intermediate layers are used to prevent any possible crosstalk between the two crossing lines. Although the multilayer approach proves to be more robust [6], the majority of designs employ the coplanar one; that is in fact one of the most praised features of classic QCA.

Coplanar crossings in tQCA are not possible, but multilayer crossings are, as it has been presented recently [7]. Here we go a step further, by presenting a wire crossing that is synchronized, i.e. the two wires employ such clocking schemes (fig 3) that the outputs have the same effective delay. In addition the clocking schemes allow for a two-layer design, in other words removing the requirement for additional layers, whose sole purpose is to prevent possible crosstalk. Crosstalk is prevented with a clever clocking scheme.

Figure 4 presents a two-layer synchronized wire crossing that achieves the most compact wire crossing possible. Typically it will be employed when two wires running parallel to one another have to be swapped. As already stated, there are only two layers in this design, with the inter-layer distance being equal to that between neighbouring cells. Research showed that this inter-layer distance is also the most robust one.

The total delay of the crossing is one clock cycle. The four phases are used so as to keep the distance between active cells as large as possible. Active cells on the two layers are never directly one over the other, although this would not present a real issue as long as enough cells are active in the same instant. The lower line, marked X1, travels in a diagonal fashion on the lower layer, achieved in one clock cycle (four phases), with blocks of two cells, so that the same state that is input to the first cell appears on the last cell, marked Y1. The upper line, marked X2, travels fist to the upper layer then in a diagonal fashion downwards and back to the lower layer, all again in one clock cycle.

It has to be noted that when moving from one layer to the other, the cell state propagates in an alternating fashion, state A becomes B, and vice versa, as well as state C becomes D and vice versa. When wire crossing is taking place this has no real effect, as eventually the state will be once more alternated upon moving back to the original layer. In the case when processing has to be performed on different layers, however, this fact has to be kept in mind. For states C and D it presents no problem, as they both represent the same logic value and alternating between the two states is achieved through simple addition of another adjacent cell. For states A and B, which represent two opposite logic values (-1 and 1 respectively), this however means adding an inverter (which in its simplest form could be just one cell displaced diagonally) or designing the processing element based on an inverted input value.

Our current research is devoted to the study of synchronized two-layer wire crossings that consume fewer clock cycles as well as tile based solutions, what we find to be one of the more promising approaches for QCA design in general.

References

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Figures

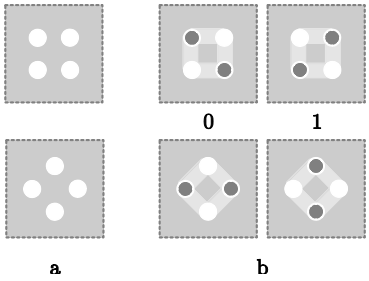

Fig 1. The binary quantum-dot cell, the rotated binary quantum dot cell (a), and the representation of the binary logic values (b).

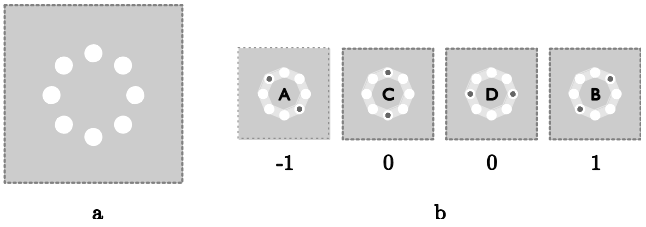

Fig 2. The ternary quantum-dot cell (a), and the representation of the ternary logic values (b).

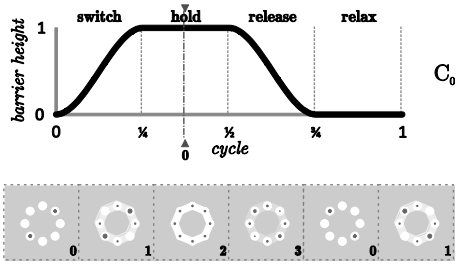

Fig 3. The clock cycle governing the pipeline transmission through a quantum-dot cellular automaton. It is based on four phases, switch (0-¼), hold (¼-½), release (½-¾) and relax (¾-1). Indexes 0-3 indicate clock zones, governed by a phase shifted original clock signal C_0, so that when a cell in clock zone 0 is in the hold phase, a cell in clock zone 1 is in the switch phase.

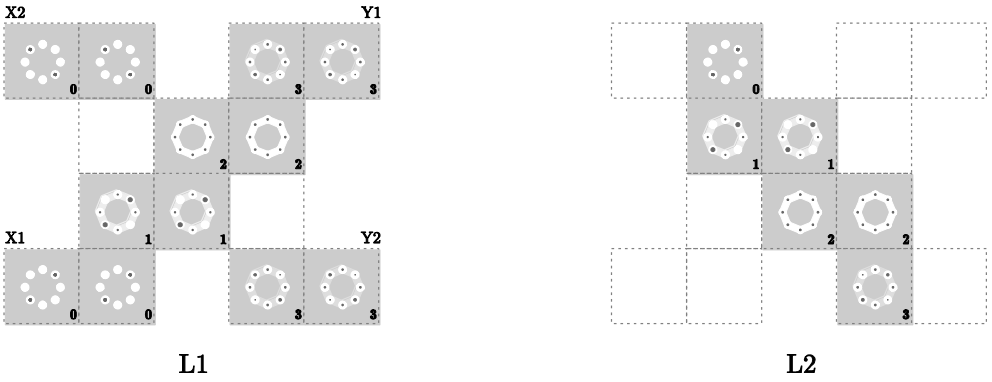

Fig 4. The two-layer synchronized wire crossing in ternary quantum-dot cellular automata.